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10/707,342	12/05/2003	Zhidan Li Tolt	nanogate120303	1341

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EXAMINER
FENTY, JESSE A

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 03/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,342	TOLT, ZHIDAN LI	
	Examiner	Art Unit	
	Jesse A. Fenty	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *38-75* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *64-68,70 and 75* is/are allowed.

6)☒ Claim(s) *38-50,53,54,57-63,69 and 71-74* is/are rejected.

7)☒ Claim(s) *51,52,55 and 56* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 39-42, 45-47 and 49 are rejected under 35 U.S.C. 102(e) as being anticipated by Raina et al. (U.S. Patent No. 6,635,983 B1).

In re claim 39, Raina (e.g., Figs. 4, 5) discloses a semiconductor device comprising:

a cathode electrode (118) disposed on a substrate (116) the cathode electrode for providing a source of electrons;

an emitter layer (122) disposed over said cathode electrode and formed from a composition of an embedding material and one or a plurality of nano-structures embedded therein, the emitter layer having a surface, portions of the nano-structures protruding above the surface to emit electrons;

an insulator (126) disposed over the emitter layer, the insulator having one or a plurality of apertures, each exposing at least the ends of the nano-structures in the emitter layer; and

a gate electrode (124) disposed over the insulator and having one or a plurality of apertures,

wherein each aperture exposes a single nano-structure and is concentrically self-aligned with the end of the nano-structure, the gate electrode being operative to control the emission of electrons through the apertures from the exposed nano-structures.

wherein the nano-structures have a coating for enhanced field emission performance.

In re claim 40, Raina discloses the device of claim 39, wherein the nano-structures are substantially vertical.

In re claim 41, Raina discloses the device of claim 39, wherein said nano-structures are individually spaced apart.

In re claim 42, Raina discloses the device of claim 39, wherein said emitter-to-gate distance for each nano-structure is substantially less than one micron (as can be gleaned from the drawing figures and the disclosed thicknesses of the gate layers in column 6, lines 24-27).

In re claim 45, Raina discloses the device of claim 39, wherein the apertures in the insulator expose the entire protrusion of the nano-structures in the emitting layer.

In re claim 46, Raina discloses the device of claim 39, wherein the nano-structures have at least one of their three dimensions in the nanometer range.

In re claim 47, Raina discloses the device of claim 39, wherein the nano-structures include nano-cones (column 3, lines 29-31).

In re claim 49, Raina discloses the device of claim 39, wherein the nano-structures are amorphous silicon (column 3, lines 26-28).

3. Claims 39-47, 49, 50, 53, 54, 57-63, 69 and 71-74 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee et al. (US 2005/0067935 A1).

In re claim 39, Lee (e.g., Fig. 7) discloses a semiconductor device comprising:

a cathode electrode (described in section [0021]) disposed on a substrate (12) the cathode electrode for providing a source of electrons;

an emitter layer (20) disposed over said cathode electrode and formed from a composition of an embedding material and one or a plurality of nano-structures embedded therein, the emitter layer having a surface, portions of the nano-structures protruding above the surface to emit electrons;

an insulator (26) disposed over the emitter layer, the insulator having one or a plurality of apertures, each exposing at least the ends of the nano-structures in the emitter layer; and

a gate electrode (32) disposed over the insulator and having one or a plurality of apertures,

wherein each aperture exposes a single nano-structure and is concentrically self-aligned with the end of the nano-structure, the gate electrode being operative to control the emission of electrons through the apertures from the exposed nano-structures.

In re claim 40, Lee discloses the device of claim 39, wherein the nano-structures are substantially vertical.

In re claim 41, Lee discloses the device of claim 39, wherein said nano-structures are individually spaced apart.

In re claim 42, Lee discloses the device of claim 39, wherein said emitter-to-gate distance for each nano-structure is substantially less than one micron (dimension "42", section [0030]).

In re claim 43, Lee discloses the device of claim 39, wherein the nano-structures have a surface density substantially higher than $10^6/cm^2$ (see bottom of section [0030]).

In re claim 44, Lee discloses the device of claim 39, wherein the nano-structures protrude above the surface of the emitting layer for not more than half on one micron (dimension "28", section [0030]).

In re claim 45, Lee discloses the device of claim 39, wherein the apertures in the insulator expose the entire protrusion of the nano-structures in the emitting layer.

In re claim 46, Lee discloses the device of claim 39, wherein the nano-structures have at least one of their three dimensions in the nanometer range.

In re claim 47, Lee discloses the device of claim 39, wherein the nano-structures include nano-wires.

In re claim 49, Lee discloses the device of claim 39, wherein the nano-structures comprise refractory metals or carbon (section [0025]).

In re claim 50, Lee discloses the device of claim 39, wherein the carbon includes carbon nano-tube or nano-fiber.

In re claim 53, Lee discloses the device of claim 39, wherein the embedding material is comprised of at least two layers[1] (section [0025]).

In re claim 54, Lee discloses the device of claim 39, wherein the first layer of the embedding material is conductive.

In re claim 57, Lee discloses the device of claim 39, wherein the cathode electrode is configured as a plurality of electrically isolated cathode electrodes, each for supplying an independent source of electrons;

wherein the gate electrodes is configured as a plurality of electrically isolated electrodes, each intersecting with said cathode electrodes and having one or a plurality of apertures at each intersections, each gate electrode being operative to control the emissions of electrons through the apertures along the gate electrode; and

wherein activation of a selected cathode and a selected gate electrode determines.

In re claim 58, Lee (e.g., Fig. 7) discloses a semiconductor device, comprising:

a substrate (12);

electrode means (described in section [0021]), disposed over the substrate, for providing a source of electrons;

means (20), disposed over the source means. for emitting electrons provided by the source means, the emitting means including a one or a plurality of nano-structure emitting means for providing a flow of electrons and means for supporting the nano-structure emitting means;

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[1] This limitation is broadly met by the carbide materials disclosed by Lee which comprise compounds

an insulator (26) disposed over the emitting means; and

one or a plurality of gating means (32) disposed over the insulator, for controlling the flow of electrons emitted by the nano-structure emitting means, each of said gating means arranged symmetrically relative to one of the nano-structure emitting means.

In re claim 59, Lee discloses the device of claim 58, wherein the insulator and the gating means each include one or more apertures that expose the nano-structure emitting means.

In re claim 60, Lee discloses the device of claim 58, wherein the nano-structure emitting means has at least one of its three dimensions in the nanometer range.

In re claim 61, Lee discloses the device of claim 58, wherein the carbon includes carbon nano-tube or nano-fiber.

In re claim 62, Lee discloses the device of claim 58, wherein the nano-structure emitting means is substantially vertical.

In re claim 63, Lee discloses the device of claim 58, wherein the nano-structures emitting means is substantially vertical.

In re claim 69, Lee discloses the device of claim 39, wherein said nano-structures in the emitter layer are truncated to substantially the same length, so that each exposed nano-structure in the gate aperture has substantially the same gate-to-emitter distance.

In re claim 71, Lee discloses the device of claim 39. The limitation, "wherein ... are grown ... material" is a process limitation that does not further define the structure of the invention and is not given patentable weight in terms of the final structure. Applicant

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consisting of two materials.

must claim positive structural characteristics of an invention to garner consideration for such limitations.

In re claim 72, Lee discloses the device of claim 58, wherein said supporting means is provided by embedding portion of the nano-structure emitting means.

In re claim 73, Lee discloses the device of claim 59, wherein said nano-structure emitting means each has substantially the same distance to the gating means.

In re claim 74, Lee discloses the device of claim 63, wherein the nano-structures are truncated to substantially the same length.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 38 and 48 rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (as above) in view of Duan et al. (US 2005/0079659 A1).

In re claim 38, Lee (e.g., Fig. 7) discloses a semiconductor device comprising:

a cathode electrode (described in section [0021]) disposed on a substrate (12) the cathode electrode for providing a source of electrons;

an emitter layer (20) disposed over said cathode electrode and formed from a composition of an embedding material and one or a plurality of nano-structures

embedded therein, the emitter layer having a surface, portions of the nano-structures protruding above the surface to emit electrons;

an insulator (26) disposed over the emitter layer, the insulator having one or a plurality of apertures, each exposing at least the ends of the nano-structures in the emitter layer; and

a gate electrode (32) disposed over the insulator and having one or a plurality of apertures,

wherein each aperture exposes a single nano-structure and is concentrically self-aligned with the end of the nano-structure, the gate electrode being operative to control the emission of electrons through the apertures from the exposed nano-structures.

Lee does not expressly disclose the nano-structures having a coating.

Duan (e.g., Fig. 3D) disclose a nano-wire (310) with a coating (304). Such coatings are well known in the art and it would have been obvious for one skilled in the art at the time of the invention to coat the nano-wires of Lee with an insulative coating as disclosed by Duan for the purpose, for example, of providing further insulation between conductive layers.

In re claim 48, Lee discloses the device of claim 39, but does not expressly disclose the nano-structures having a coating.

Duan (e.g., Fig. 3D) disclose a nano-wire (310) with a coating (304). Such coatings are well known in the art and it would have been obvious for one skilled in the art at the time of the invention to coat the nano-wires of Lee with an insulative coating

as disclosed by Duan for the purpose, for example, of providing further insulation between conductive layers.

Allowable Subject Matter

6. Claims 51, 52, 55 and 56 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claims 64-68, 70 and 75 are allowed.

a. The following is a statement of reasons for the indication of allowable subject matter: The semiconductor device comprising at least a cathode electrode disposed on a substrate, an emitter layer, an insulator, a gate electrode, and an anode plate including a transparent anode electrode disposed over a glass substrate and a phosphor screen disposed over the anode electrode, the anode plate being positioned opposite to said electron source with a vacuum gap disposed therebetween, is neither anticipated nor obvious over the prior art of record.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 571-272-1729. The examiner can normally be reached on 5/4-9 1st Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jesse A. Fenty

Examiner
Art Unit 2815

JEROME JACKSON
PRIMARY EXAMINER